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PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Louis L. Hsu, et al.	**Examiner:**	K. N. McLean Mayo
Serial No:	09/855,240	**Art Unit:**	2187
Filed:	May 15, 2001	**Docket:**	YOR920000660US1 (13959)
For:	HIGH SPEED EMBEDDED DRAM WITH SRAM-LIKE INTERFACE	**Dated:**	February 28, 2003

Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

AMENDMENT UNDER 1.111

Sir:

Responsive to the Office Action of November 29, 2002, please amend this patent application as follows:

IN THE CLAIMS:

Please amend claims 4, 8 and 13 as follows to obviate the rejections thereof under 35 USC 112.

4. (Amended) The high speed DRAM of claim 1, wherein a sixth data bus couples the read register to a data output from the high speed DRAM, and a seventh data bus couples a data input to the high speed DRAM to the write register.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231 on February 28, 2003.

Dated: February 28, 2003

Michelle Mustafa